What is claimed is:

1. A thin film patterning method, comprising:

a first step of preparing an inorganic material substrate;

a second step of forming an organic material pattern at a desired area of the inorganic material substrate;

a third step of forming a thin film having a different crystallization rate depending upon said inorganic material and said organic material; and

a fourth step of selectively etching the thin film in accordance with said crystallization rate.

2. The thin film patterning method as claimed in claim 1, wherein said third step includes:

forming a transparent conductive film having a different binding structure depending upon a type of said material.

3. The thin film patterning method as claimed in claim 2, wherein said step of forming the transparent conductive film includes:

forming the transparent conductive film on the inorganic material substrate while heating the inorganic material substrate at a temperature range of about 100°C to 200°C.

4. The thin film patterning method as claimed in claim 2, wherein said transparent conductive film is formed into an amorphous substance on the inorganic material substrate while being formed a crystalline substance on the organic material pattern.

5. The thin film patterning method as claimed in claim 4,

wherein said fourth step includes:

selectively etching out the amorphous transparent conductive film on the organic material pattern using an etchant for amorphous substance.

6. The thin film patterning method as claimed in claim 1, further comprising:

a step of forming a crystallization catalyst layer at the remaining area excluding an area where the organic material pattern is formed, between said second step and said third step, so as to accelerate a crystallization of the thin film.

7. The thin film patterning method as claimed in claim 6, wherein said crystallization catalyst layer includes at least one of refractory metals such as Ni, Cu, In, Sn, Mo, Tn, W, Cr and Hf.

8. The thin film patterning method as claimed in claim 7, wherein said crystallization catalyst layer is formed such that atoms of said metals has a distribution scattered on a sparsely basis.

9. The thin film patterning method as claimed in claim 6, wherein said second step includes:

entirely forming the organic film on the inorganic material substrate; and

patterning the organic film by an etching process using a photo-resist pattern formed by the photolithography.

10. The thin film patterning method as claimed in claim 9, wherein said step of forming the crystallization catalyst

layer includes:

entirely forming the crystallization catalyst layer on said substrate in which the photo-resist pattern is formed on the organic material pattern; and

removing the crystallization catalyst layer on the photo-resist pattern along with the photo-resist pattern.

11. A method of patterning a transparent conductive film, comprising:

a first step of preparing an inorganic material substrate;

a second step of forming an organic film on said substrate; and

a third step of forming a transparent conductive film making an interface with the organic film on a substrate at the remaining area including an area where the organic film is formed.

12. The method as claimed in claim 11, wherein said second step includes:

entirely forming the organic film on said substrate; and

patterning the organic film by an etching process using a photo-resist pattern formed by the photolithography.

13. The method as claimed in claim 11, wherein said third step includes:

entirely forming the transparent conductive film on said substrate on which the organic film is formed; and

selectively etching the transparent conductive film on the organic film depending upon a crystallization rate of the transparent conductive film.

14. The method as claimed in claim 13, wherein said step of forming the transparent conductive film includes:

entirely forming the transparent conductive film while heating said substrate at a temperature range of about 100°C to 200°C.

15. The method as claimed in claim 14, wherein said transparent conductive film is formed into an amorphous substance on the inorganic material substrate while being formed a crystalline substance on the organic film.

16. The method as claimed in claim 15, wherein said step of selectively etching the transparent conductive film includes:

selectively etching out the amorphous transparent conductive film on the organic film using an etchant for amorphous substance.

17. The method as claimed in claim 16, wherein an etching ratio of the amorphous transparent conductive film to the crystalline transparent conductive film is controlled by differentiating a content of an oxalic acid contained in the etchant for amorphous substance.

18. The method as claimed in claim 15, wherein said transparent conductive film is formed to have a thickness of about 500 Å or less.

19. The method as claimed in claim 11, wherein said transparent conductive film is formed from at least one of ITO, TO, IZO and

SnO_2.

20. The method as claimed in claim 12, further comprising:

a step of forming a crystallization catalyst layer on the inorganic material substrate at the remaining area excluding an area where the organic film is formed, between said second step and said third step, so as to accelerate a crystallization of the transparent conductive film.

21. The method as claimed in claim 20, wherein said crystallization catalyst layer includes at least one of refractory metals such as Ni, Cu, In, Sn, Mo, Tn, W, Cr and Hf.

22. The method as claimed in claim 21, wherein said crystallization catalyst layer is formed such that atoms of said metals has a distribution scattered on a sparsely basis.

23. The method as claimed in claim 20, wherein said step of forming the crystallization catalyst layer includes:

entirely forming the crystallization catalyst layer on said substrate in which the photo-resist pattern is formed on the organic film; and

removing the crystallization catalyst layer on the photo-resist pattern along with the photo-resist pattern.

24. A display device having a transparent conductive film, comprising:

a substrate;

an organic film formed at a desired area of the substrate; and

a transparent conductive film formed at the remaining area including an area where the organic film is formed in such a manner to make an interface with the organic film.

25. The display device as claimed in claim 24, wherein said substrate is formed from an inorganic material.

26. The display device as claimed in claim 25, wherein the transparent conductive film formed on the inorganic material substrate has a crystalline structure.

27. The display device as claimed in claim 24, wherein said transparent conductive film is formed to have a thickness of about 500 Å or less.

28. The display device as claimed in claim 24, wherein said transparent conductive film is formed from at least one of ITO, TO, IZO and SnO_2.

29. The display device as claimed in claim 24, further comprising:

a crystallization catalyst layer formed at the remaining area excluding an area where the organic film is formed so as to accelerate a crystallization of the transparent conductive film.

30. The display device as claimed in claim 29, wherein said crystallization catalyst layer is formed such that metal atoms of at least one of refractory metals such as Ni, Cu, In, Sn, Mo, Tn, W, Cr and Hf have a distribution scattered on a sparsely basis.

31. A thin film transistor substrate for a display device, comprising:

a gate line;

a data line crossing the gate line with having a gate insulating film therebetween to define a pixel area;

a thin film transistor formed at an intersection between the gate line and the data line;

a protective film covering the gate line, the data line and the thin film transistor except for said pixel area; and

a pixel electrode formed at said pixel area in such a manner to make an interface with the protective film and connected to the thin film transistor.

32. The thin film transistor substrate as claimed in claim 31, wherein said protective film is any one of an organic insulating film, an inorganic insulating film and an inorganic/organic insulating film having a double-layer structure.

33. The thin film transistor substrate as claimed in claim 32, wherein said pixel electrode is formed to cover an area until the side surface of the protective film when the protective film includes the inorganic insulating film.

34. The thin film transistor substrate as claimed in claim 31, further comprising:

a semiconductor layer formed along the data line on the gate insulating film to be included in the thin film transistor.

35. The thin film transistor substrate as claimed in claim 31, further comprising:

a gate pad lower electrode formed from the same material as the gate line;

a contact hole passing through the protective film and the gate insulating film to expose the gate pad lower electrode; and

a gate pad portion formed from the same material as the pixel electrode and including a gate pad upper electrode connected to the gate pad lower electrode through the contact hole.

36. The thin film transistor substrate as claimed in claim 35, wherein the gate pad upper electrode makes an interface with the protective film.

37. The thin film transistor substrate as claimed in claim 35, wherein said gate pad upper electrode is coated onto the side surface of the inorganic insulating film when the protective film includes the inorganic insulating film.

38. The thin film transistor substrate as claimed in claim 31, further comprising:

a data pad lower electrode formed from the same material as the data line;

a contact hole passing through the protective film to expose the data pad lower electrode; and

a data pad portion formed from the same material as the pixel electrode and including a data pad upper electrode connected to the data pad lower electrode through the contact hole.

39. The thin film transistor substrate as claimed in claim 38, wherein the data pad upper electrode makes an interface with the protective film.

40. The thin film transistor substrate as claimed in claim 38, wherein said data pad upper electrode is coated onto the side surface of the inorganic insulating film when the protective film includes the inorganic insulating film.

41. The thin film transistor substrate as claimed in claim 38, wherein said contact hole passes through the data pad lower electrode, and said data pad upper electrode makes a side contact with the data pad lower electrode through said contact hole.

42. The thin film transistor substrate as claimed in claim 41, further comprising:

a storage lower electrode made by a portion of the gate line; and

a storage capacitor formed from the same material as the data line on the gate insulating film in such a manner to overlap with the storage lower electrode and including a storage upper electrode making a side contact with the pixel electrode.

43. The thin film transistor substrate as claimed in claim 32, wherein said organic insulating film is formed from at least one of an acrylic organic compound, BCB and PFCB.

44. The thin film transistor substrate as claimed in claim

31, wherein said pixel electrode is formed to have a thickness of about 500 Å or less.

45. The thin film transistor substrate as claimed in claim 31, wherein said pixel electrode is formed from at least one of ITO, TO, IZO and SnO_2.

46. The thin film transistor substrate as claimed in claim 31, wherein said pixel electrode makes a side contact with a drain electrode of the thin film transistor protruded toward said pixel area.

47. The thin film transistor substrate as claimed in claim 31, further comprising:

a crystallization catalyst layer formed at the lower portion of the pixel electrode positioned at the remaining area excluding an area where the organic film is formed.

48. The thin film transistor substrate as claimed in claim 47, wherein said crystallization catalyst layer is formed such that metal atoms of at least one of refractory metals such as Ni, Cu, In, Sn, Mo, Tn, W, Cr and Hf have a distribution scattered on a sparsely basis.

49. A method of fabricating a thin film transistor substrate for a display device, comprising:

a first step of forming a gate line on a substrate;

a second step of forming a gate insulating film covering the gate line;

a third step of forming a semiconductor layer at a desired area on the gate insulating film;

a fourth step of forming a data line crossing the gate line, a source electrode connected to the data line and a drain electrode opposed to the source electrode on the gate insulating film;

a fifth step of forming a protective film in such a manner to cover the gate line, the data line, the source electrode and the drain electrode; and

a sixth step of forming a pixel electrode making an interface with the protective film at the remaining area excluding an area where the protective film is formed and connected to the drain electrode.

50. The method as claimed in claim 49, further comprising the steps of:

providing a gate pad lower electrode formed from the same material as the gate line;

providing a contact hole passing through the protective film and the gate insulating film to expose the gate pad lower electrode; and

providing a gate pad upper electrode formed from the same material as the pixel electrode and connected to the gate pad lower electrode through said contact hole.

51. The method as claimed in claim 49, further comprising the steps of:

providing a data pad lower electrode formed from the same material as the data line on the gate insulating film;

providing a contact hole passing through the protective film to expose the data pad lower electrode; and

providing a data pad upper electrode formed from the same material as the pixel electrode and connected to the data pad

lower electrode through said contact hole.

52. The method as claimed in claim 49, further comprising the step of:

providing a storage upper electrode formed from the same material as the data line on the gate insulating film in such a manner to overlap with a portion of the gate line and making a side contact with the pixel electrode.

53. The method as claimed in claim 49, wherein said protective film is any one of an organic insulating film, an inorganic insulating film and an inorganic/organic insulating film having a double-layer structure.

54. The method as claimed in claim 53, wherein said sixth step includes:

coating the transparent conductive film formed into an amorphous substance on the protective film including an organic material while being formed into a crystalline substance at the remaining area formed from an inorganic material; and

selectively etching the amorphous transparent conductive film on the protective film using an etchant for amorphous substance to thereby leave only the crystalline transparent conductive film.

55. The method as claimed in claim 49, further comprising:

a step of forming a crystallization catalyst layer at the remaining area excluding an area where the protective film is formed between said fifth step and said sixth step.

56. The method as claimed in claim 55, wherein said fifth step includes:

entirely forming the protective film on said substrate; and

patterning the protective film by an etching process using a photo-resist pattern formed by the photolithography.

57. The method as claimed in claim 56, wherein said step of forming the crystallization catalyst layer includes:

entirely forming the crystallization catalyst layer on said substrate in which the photo-resist pattern is formed on the protective film; and

removing the crystallization catalyst layer on the photo-resist pattern along with the photo-resist pattern.

58. The method as claimed in claim 55, wherein said crystallization catalyst layer is formed such that metal atoms of at least one of refractory metals such as Ni, Cu, In, Sn, Mo, Tn, W, Cr and Hf have a distribution scattered on a sparsely basis.

59. A method of fabricating a thin film transistor substrate for a display device, comprising:

a first mask process of forming a gate line using a first mask after forming a gate metal layer on a substrate;

a process of disposing a gate insulating film, an amorphous silicon layer, an amorphous silicon layer doped with an impurity and a source/drain metal layer;

a second mask process of patterning the source/drain metal layer, the amorphous silicon layer doped with said impurity and the amorphous silicon layer using a second mask

to thereby provide a data line, a source electrode, a drain electrode and a semiconductor layer;

a third mask process of etching out a protective film at a pixel area defined by an intersection between the gate line and the data line and the gate insulating film using a third mask after forming the protective film; and

a process of selectively etching out a transparent conductive film on the protective film after forming the transparent conductive film to thereby provide a pixel electrode making an interface with the protective film and connected to the drain electrode.

60. The method as claimed in claim 59, wherein said second mask process includes:

forming a photo-resist pattern having a different thickness on a source/drain metal layer using said partially transmitting mask;

patterning the source/drain metal layer, the amorphous silicon layer doped with said impurity and the amorphous silicon layer using the photo-resist pattern to thereby provide the data line, the drain electrode integral to the source electrode and the semiconductor layer;

ashing the photo-resist pattern to remove a relatively thin photo-resist pattern;

disconnecting the source electrode from the drain electrode through a portion at which said thin photo-resist pattern is removed and removing the amorphous silicon layer doped with said impurity; and

removing the remaining photo-resist pattern.

61. The method as claimed in claim 59, further comprising the

steps of:

providing a gate pad lower electrode formed from the same material as the gate line by the first mask process;

providing a contact hole passing through the protective film and the gate insulating film to expose the gate pad lower electrode by the third mask process; and

providing a gate pad upper electrode formed from the same material as the pixel electrode and connected to the gate pad lower electrode through said contact hole.

62. The method as claimed in claim 59, further comprising the steps of:

providing a data pad lower electrode formed from the same material as the data line on the gate insulating film by the second mask process;

providing a contact hole passing through the protective film to expose the data pad lower electrode; and

providing a data pad upper electrode formed from the same material as the pixel electrode and connected to the data pad lower electrode through said contact hole.

63. The method as claimed in claim 59, further comprising the step of:

providing a storage upper electrode formed from the same material as the data line on the gate insulating film in such a manner to overlap with a portion of the gate line and making a side contact with the pixel electrode by the second mask process.

64. The method as claimed in claim 59, wherein said protective film is formed from an organic insulating film.

65. The method as claimed in claim 59, wherein said protective film is formed from an inorganic insulating film.

66. The method as claimed in claim 65, wherein said pixel electrode is formed to cover an area until the side surface of the inorganic insulating film.

67. The method as claimed in claim 59, wherein said protective film is formed from a double layer of an inorganic insulating film and an organic insulating film.

68. The method as claimed in claim 67, wherein said pixel electrode is formed to cover an area until the side surface of the inorganic insulating film.

69. The method as claimed in claim 61, wherein said gate pad upper electrode makes an interface with the protective film.

70. The method as claimed in claim 61, wherein said gate pad upper electrode is coated onto the side surface of the inorganic insulating film when the protective film includes the inorganic insulating film.

71. The method as claimed in claim 62, wherein said data pad upper electrode makes an interface with the protective film.

72. The method as claimed in claim 62, wherein said data pad upper electrode is coated onto the side surface of the inorganic insulating film when the protective film includes the inorganic insulating film.

73. The method as claimed in claim 62, wherein said contact hole is formed to pass through the data pad lower electrode such that the data pad upper electrode makes a side contact with the data pad lower electrode.

74. The method as claimed in claim 59, wherein said step of forming the pixel electrode includes:

coating the transparent conductive film formed into an amorphous substance on the protective film including an organic material while being formed into at the remaining area formed from an inorganic material; and

selectively etching the amorphous transparent conductive film on the protective film using an etchant for amorphous substance to thereby leave only the crystalline transparent conductive film.

75. The method as claimed in claim 74, wherein the protective film including said organic material is formed from at least one of an acrylic organic compound, BCB and PFCB.

76. The method as claimed in claim 74, further comprising the step of:

removing the organic material protective film making an interface with the crystalline transparent conductive film when the protective film is a built layer of the inorganic material protective film and the organic material protective film.

77. The method as claimed in claim 76, wherein said organic material protective film is made from an organic material

including a photosensitive resin.

78. The method as claimed in claim 74, further comprising the step of:

heating the substrate on which the protective film is formed at a temperature range of about 100°C to 200°C while coating the transparent conductive film.

79. The method as claimed in claim 74, wherein said transparent conductive film is formed to have a thickness of about 500 Å or less.

80. The method as claimed in claim 74, wherein said pixel electrode is formed from at least one of ITO, TO, IZO and SnO_2.

81. The method as claimed in claim 74, wherein an etching ratio of the amorphous transparent conductive film to the crystalline transparent conductive film is controlled by differentiating a content of an oxalic acid contained in the etchant for amorphous substance.

82. The method as claimed in claim 74, wherein said etchant for amorphous substance contains an oxalic acid at a range of 3 to 5 weight%.

83. The method as claimed in claim 74, wherein said pixel electrode makes a side contact with the drain electrode protruded toward said pixel area.

84. The method as claimed in claim 59, further comprising the step of:

forming a crystallization catalyst layer at the remaining area excluding an area where the protective film is formed between said second mask process and said third mask process.

85. The method as claimed in claim 84, wherein said step of forming the protective film includes:

entirely forming the protective film on said substrate; and

patterning the protective film by an etching process using a photo-resist pattern formed by the photolithography.

86. The method as claimed in claim 85, wherein said step of forming the crystallization catalyst layer includes:

entirely forming the crystallization catalyst layer on said substrate in which the photo-resist pattern is formed on the protective film; and

removing the crystallization catalyst layer on the photo-resist pattern along with the photo-resist pattern.

87. The method as claimed in claim 84, wherein said crystallization catalyst layer is formed such that metal atoms of at least one of refractory metals such as Ni, Cu, In, Sn, Mo, Tn, W, Cr and Hf have a distribution scattered on a sparsely basis.